

REMARKS

Claims 10-14 are pending in the application. Claims 10 and 13 have been amended, Claims 16 and 17 have been canceled, leaving Claims 10-15 for consideration upon entry of the present amendment.

Support for the amendment to Claims 10 and 13 can at least be found in Figs. 3 and 4(c)-4(e) and the corresponding description in the specification.

No new matter has been introduced by these amendments. Reconsideration and allowance of the claims are respectfully requested in view of the above amendments and the following remarks.

Claim Rejections Under 35 U.S.C. § 103(a)

Claims 10-12 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Yamazaki et al. (U.S. Patent No. 5,917,225) in view of Tanabe et al. (U.S. PG-Pub 2002/0072158). Claims 10-12 stand rejected also under 35 U.S.C. § 103(a) as being allegedly unpatentable over Ogawa (JP 5-335578) in view of Tanabe. Additionally, claims 13-15 are rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over Yamazaki in view of Tanabe. Claims 13-15 are additionally rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over Ogawa in view of Tanabe.

For an obviousness rejection to be proper, the Examiner must meet the burden of establishing that all elements of the invention are disclosed in the prior art; and that the prior art relied upon, coupled with knowledge generally available in the art at the time of the invention, must contain some suggestion or incentive that would have motivated the skilled artisan to modify a reference or combined references. *In re Fine*, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988); *In Re Wilson*, 165 U.S.P.Q. 494, 496 (C.C.P.A. 1970); *Amgen v. Chugai Pharmaceuticals Co.*, 927 U.S.P.Q.2d 1016, 1023 (Fed. Cir. 1996).

Claims 10-15 comprise, *inter alia*, the following limitations: "said second gate insulating film has a smaller film thickness in a region not covered with said gate electrode than that in said region covered with said gate electrode, along a channel length direction of a channel region of said thin film transistor formed in said semiconductor film, from an end position of said gate electrode

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covering said second gate insulating film; said second gate insulating film covers said first gate insulating film in said region not covered with said gate electrode in which said second gate insulating film has said smaller film thickness; and said second insulating film has a smaller film thickness from an end position of said gate electrode covering said second insulating film.”

In the presently claimed invention, the gate insulating film is made of a first gate insulating film and a second gate insulating film. The second gate insulating film, which is the gate insulating film nearer to the gate electrode, has a smaller film thickness in a region not covered with the gate electrode than that in a region covered with the gate electrode from an end position of the gate electrode. More specifically, the second gate insulating film has a smaller film thickness “along a channel length direction of a channel region of said thin film transistor formed in said semiconductor film” in a region not covered with the gate electrode, from an end position of the gate electrode.

The Examiner states “Tanabe discloses (see fig. 3, par. 0077 and claim 1) a silicon nitride insulating film 6 with a smaller film thickness in a region not covered with a gate electrode 7 than a silicon nitride insulating film in a region covered with said gate electrode”. (O.A., page 3). Applicant respectfully disagrees, and asserts that the thickness of the “silicon nitride insulating film 6” in Tanabe is uniform throughout the region not covered with the gate electrode 7 and the region covered with the gate electrode 7. Tanabe disclose a configuration where a part of the first gate insulating film 5 below the insulating film 6 is removed, the total thickness of the first and second gate insulating films 5 and 6 is smaller in a region in which the first gate insulating film 5 is removed.

The Examiner also states “Tanabe discloses a second insulating film having a smaller film thickness from an end position of said gate electrode covering said second insulating film”. (O.A., page 3). Applicant respectfully disagrees with this assertion. There is no description in Tanabe of the thickness of the second gate insulating film being smaller from an end position of the gate electrode. Rather, there is only a description that the total thickness of the first and second gate insulating films is smaller at an outer position than the end position of the gate electrode along the channel length direction, that is, an outer position than the channel region of the TFT. As described above, the thickness of the second gate insulating film is the same in the region not

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covered with the gate electrode and in the region covered with the gate electrode. Tanabe discloses, the total thickness of the first and second gate insulating films is reduced along the channel width direction rather than the channel length direction by partially removing the first gate insulating film in a region covered with the gate electrode.

Additionally, Yamazaki fails to disclose that the thickness of the second gate insulating film is smaller in a region not covered with the gate electrode along the "channel length direction" from an end position of the gate electrode. Rather, Yamazaki discloses a configuration where the second gate insulating film is etched and completely removed at an outer position along the channel length direction than the end position of the gate electrode, as shown in Figs. 1(C) and 1(D).

Furthermore, Ogawa fails to disclose that the thickness of the second gate insulating film is smaller in a region not covered with the gate electrode along the "channel length direction" from an end position of the gate electrode. Rather, Ogawa discloses a configuration where the second (upper) gate insulating film is completely removed in a region not covered with the gate electrode.

Although the Examiner maintains that it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate Tanabe's teaching with Yamazaki's device or with Ogawa's device, even if combined, none of the citations disclose that the "second gate insulating film" is maintained with a smaller thickness in a region not covered with the gate electrode rather than the second gate insulating film being completely removed. Furthermore, neither Tanabe, Yamazaki, nor Ogawa disclose a second gate insulating film that has a smaller film thickness "in a region not covered with said gate electrode than that in a region covered with said gate electrode, along a channel length direction of a channel region of said thin film transistor formed in said semiconductor film, from an end position of said gate electrode covering said second gate insulating film".

In the presently claimed invention, the thickness of the second gate insulating film is reduced from the end position of the gate electrode along the channel length direction. In other words, the channel length, the gate electrode width along the channel length direction, and the thick thickness region of the second gate insulating film match each other and occurrence of variation in characteristics of transistors is reduced. In addition, when an impurity is doped into the

semiconductor film using the gate electrode as a mask, the impurity is doped into the semiconductor film through the second and first gate insulating films, and, because the thickness of the second gate insulating film is smaller in the impurity doping region, the energy necessary for doping can be reduced even when a layered structure of the first and second gate insulating films is employed.

Moreover, by maintaining the second gate insulating film rather than completely removing the second gate insulating film in the impurity doping region, it is possible to reliably prevent intrusion, into the semiconductor film, of contaminants other than the impurity to be intentionally doped even before the interlayer insulating film is formed covering the gate electrode. In Yamazaki and Ogawa in which the second gate insulating film is completely removed, such an advantage cannot be obtained. Moreover, Yamazaki and Ogawa fail to disclose or even suggest the necessity for obtaining such an advantage. Therefore, a person with ordinary skill in the art would not be motivated to partially maintain the second gate insulating film based on these citations.

As described above, Tanabe does not disclose or teach partially removing the second gate insulating film. Rather, Tanabe discloses a configuration in which the first gate insulating film is completely removed in a partial region. Therefore, even when Yamazaki or Ogawa is combined with Tanabe, only a structure in which the first gate insulating film or the second gate insulating film is completely removed can be obtained, and, thus, the present invention cannot be viewed as obvious from these citations.

It is believed that the foregoing remarks fully comply with the Office Action and that the claims herein should now be allowable to Applicant. Accordingly, reconsideration and allowance are requested.

If there are any additional charges with respect to this Amendment or otherwise, please charge them to Deposit Account No. 06-1130.

Respectfully submitted,

CANTOR COLBURN LLP

By 

Joel T. Charlton

Registration No. 52,721

Date: March 1, 2006
Telephone (404) 607-9991
Facsimile (404) 607-9981
Customer No.: 23413

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